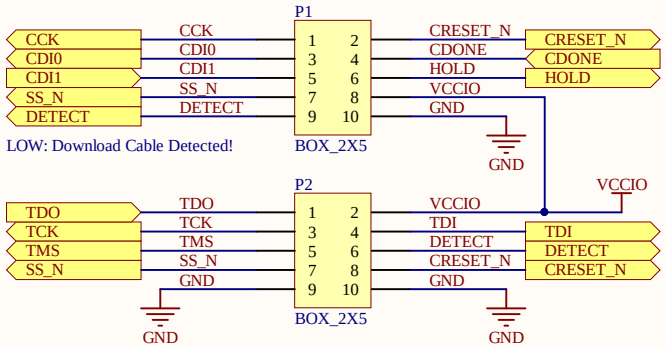
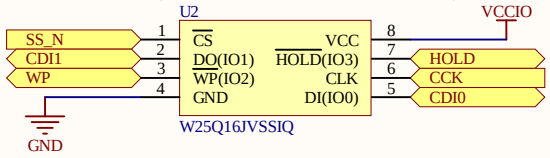
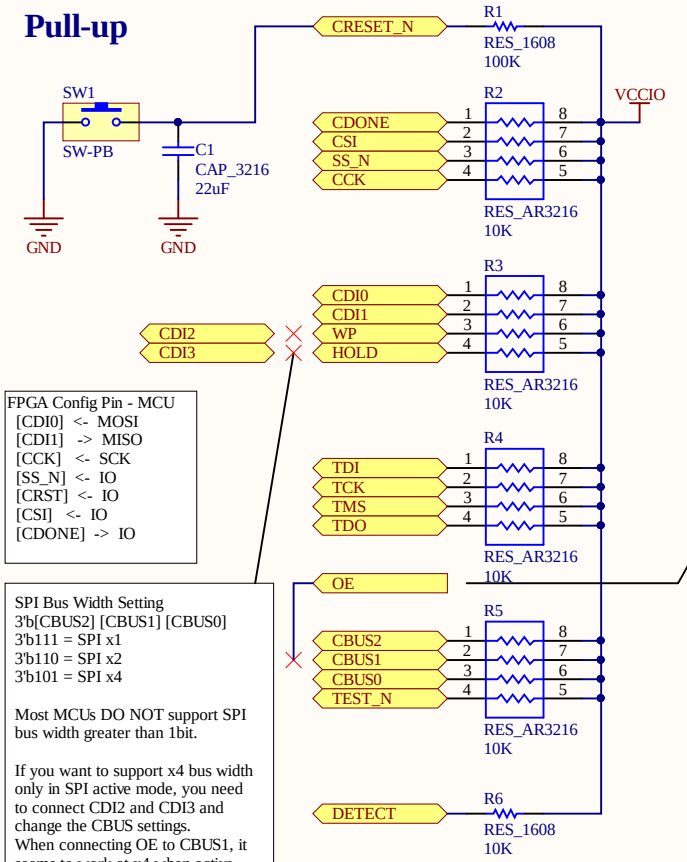
SPI / JTAG Header



SPI Flash (for SPI Active Mode)



Pull-up



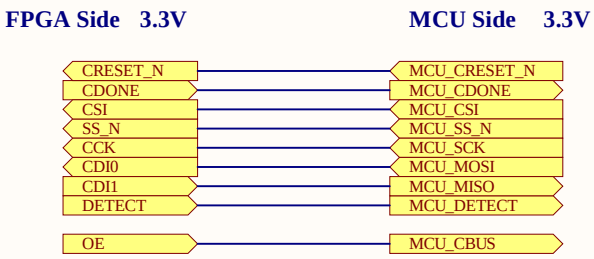
FPGA Config Pin - MCU
[CDI0] <- MOSI
[CDI1] -> MISO
[CCK] <- SCK
[SS_N] <- IO
[CRST] <- IO
[CSI] <- IO
[CDONE] -> IO

SPI Bus Width Setting
3'b[CBUS2] [CBUS1] [CBUS0]
3'b111 = SPI x1
3'b110 = SPI x2
3'b101 = SPI x4

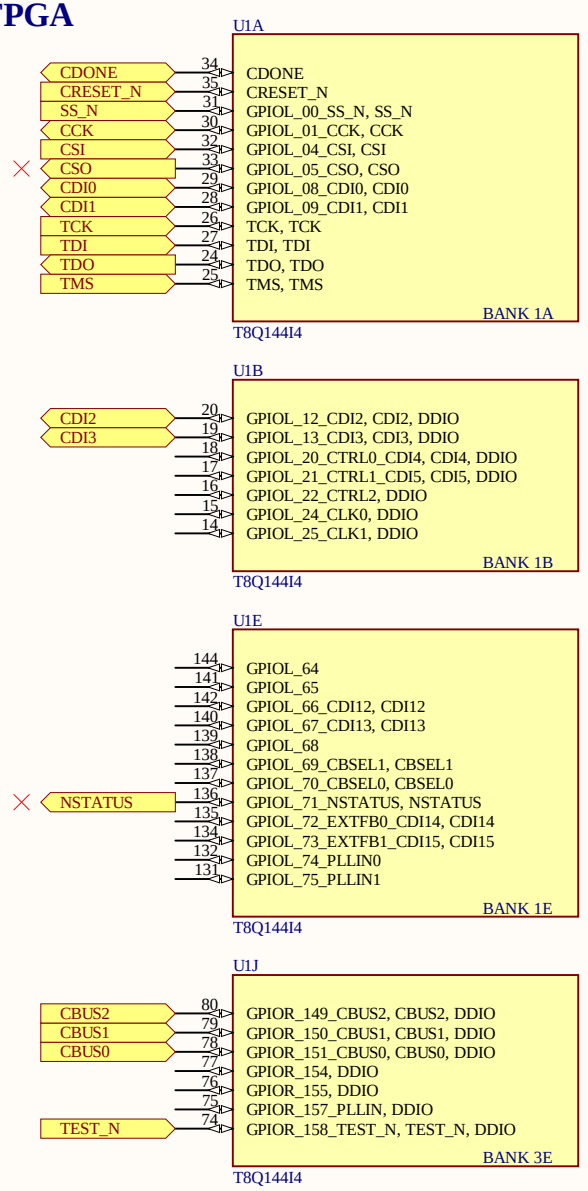
Most MCUs DO NOT support SPI bus width greater than 1bit.

If you want to support x4 bus width only in SPI active mode, you need to connect CDI2 and CDI3 and change the CBUS settings.
When connecting OE to CBUS1, it seems to work at x4 when active and x1 when passive.

Opt : MCU Interface (for SPI Passive Mode x1)



FPGA



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